

## Power Logic 12-CHANNEL SHIFT REGISTER LED DRIVER

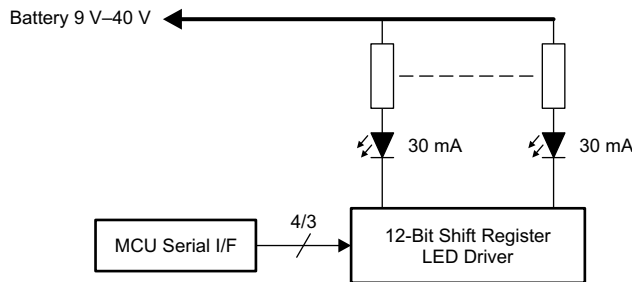
Check for Samples: [TLC6C5912-Q1](#)

### FEATURES

- Wide  $V_{CC}$  From 3 V to 5.5 V
- Output Maximum Rating of 40 V
- Twelve Power DMOS Transistor Outputs of 50-mA Continuous Current with  $V_{CC} = 5$  V
- Thermal Shutdown Protection
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption
- Slow Switching Time ( $t_r$  and  $t_f$ ), Which Helps Significantly With Reducing EMI
- 20-Pin TSSOP-PW Package
- 20-Pin DW Package

### APPLICATIONS

- Instrumentation Cluster
- Tell-Tale Lamps
- LED Illumination and Control



**Figure 1. Typical Application Schematic**

### DESCRIPTION

The TLC6C5912-Q1 is a monolithic, medium-voltage, low-current power 12-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear (CLR) is high. A low on CLR clears all registers in the device. Holding the output enable ( $\overline{G}$ ) high holds all data in the output buffers low, and all drain outputs are off. Holding  $\overline{G}$  low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. The device contains a built-in thermal shutdown protection.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50 mA continuous sink-current capabilities when  $V_{CC} = 5$  V. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2000 V of ESD protection when tested using the human-body model and the 200-V machine model.

The TLC6C5912-Q1 characterization is for operation over the operating ambient temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

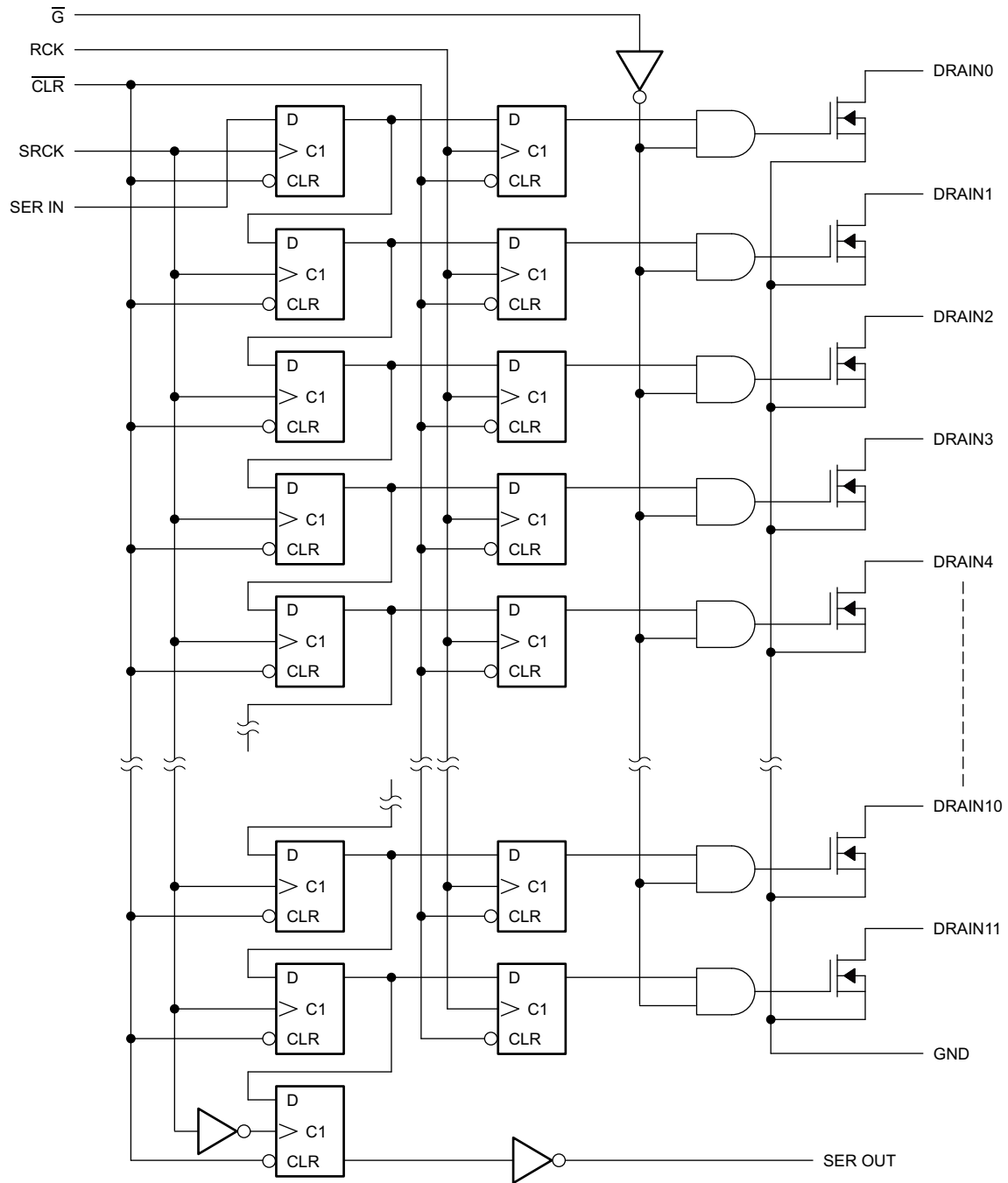


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**LOGIC DIAGRAM (Positive Logic)**



**Figure 2. Logic Diagram of TLC6C5912-Q1**

**ORDERING INFORMATION**

LABEL	PACKAGE	DESCRIPTION	ORDERABLE PART#	STATUS
TLC6C5912	TSSOP – PW-20	12-bit shift register LED driver	TLC6C5912QPWRQ1	Active
TLC6C5912	DW-20	12-bit shift register LED driver	TLC6C5912QDWRQ1	Preview

**ABSOLUTE MAXIMUM RATINGS**

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE	UNIT
V <sub>CC</sub> Logic supply voltage	8	V
V <sub>I</sub> Logic input-voltage range	–0.3 to 8	V
V <sub>DS</sub> Power DMOS drain-to-source voltage	42	V
Continuous total dissipation	See Thermal Information table	
ESD <sup>(2)</sup> Electrostatic Discharge HBM	2	kV
Top Operating ambient temperature	125	°C
T <sub>S</sub> Storage temperature range	–55 to 165	°C
T <sub>J</sub> Operating junction temperature range	–40 to 150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>	TLC6C5912-Q1		UNIT
	PW	SOIC	
	20 PINS	20 PINS	
θ <sub>JA</sub> Junction-to-ambient thermal resistance	114.8	81.2	°C/W
θ <sub>JCtop</sub> Junction-to-case (top) thermal resistance	44.1	45.4	°C/W
θ <sub>JB</sub> Junction-to-board thermal resistance	61.3	49.1	°C/W
ψ <sub>JT</sub> Junction-to-top characterization parameter	4.7	17.5	°C/W
ψ <sub>JB</sub> Junction-to-board characterization parameter	60.8	48.6	°C/W
θ <sub>JCbot</sub> Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**RECOMMENDED OPERATING CONDITIONS**

	MIN	MAX	UNIT
V <sub>CC</sub> Supply voltage	3	5.5	V
V <sub>IH</sub> High-level input voltage	2.4		V
V <sub>IL</sub> Low-level input voltage		0.7	V
t <sub>SU</sub> Setup time, SER IN high before SRCK↑	15		ns
t <sub>H</sub> Hold time, SER IN high after SRCK↑	15		ns
t <sub>w</sub> Pulse duration	40		ns
T <sub>C</sub> Operating case temperature	–40	125	°C

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Drain0 to Drain11. Drain to source voltage					40	V
$V_{OH}$	High-level output voltage, SER OUT	$I_{OH} = -20\ \mu\text{A}$	$V_{CC} = 5\text{ V}$	4.9	4.99		V
		$I_{OH} = -4\ \text{mA}$		4.5	4.69		
$V_{OL}$	Low-level output voltage, SER OUT	$I_{OH} = 20\ \mu\text{A}$	$V_{CC} = 5\text{ V}$	0.00	1	0.01	V
		$I_{OH} = 4\ \text{mA}$		0.25	0.4		
$I_{IH}$	High-level input current	$V_{CC} = 5\text{ V}$ , $V_I = V_{CC}$		0.2			$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = 5\text{ V}$ , $V_I = 0$		-0.2			$\mu\text{A}$
$I_{CC}$	Logic supply current	$V_{CC} = 5\text{ V}$ , No clock signal	All outputs off	0.1		1	$\mu\text{A}$
			All outputs on	130		170	
$I_{CC(FRQ)}$	Logic supply current at frequency	$f_{SRCK} = 5\text{ MHz}$ , $C_L = 30\ \text{pF}$ , all outputs on		300			$\mu\text{A}$
$I_{DSX}$	Off-state drain current	$V_{DS} = 30\text{ V}$ , $V_{CC} = 5\text{ V}$				0.1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}$ , $T_C = 125^\circ\text{C}$ , $V_{CC} = 5\text{ V}$				0.15	
$r_{DS(on)}$	Static drain-source on-state resistance	$I_D = 20\ \text{mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , single channel ON		6	7.4	8.6	$\Omega$
		$I_D = 50\ \text{mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , all channels ON		6.7	8.9	9.6	
		$I_D = 20\ \text{mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , single channel ON		7.9	9.3	11.2	
		$I_D = 20\ \text{mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , all channels ON		8.7	10.6	12.3	
		$I_D = 20\ \text{mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 125^\circ\text{C}$ , single channel ON		9.1	11.2	12.9	
		$I_D = 20\ \text{mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 125^\circ\text{C}$ , all channels ON		10.3	13	14.5	
		$I_D = 20\ \text{mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 125^\circ\text{C}$ , single channel ON		11.6	13.7	16.4	
		$I_D = 20\ \text{mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 125^\circ\text{C}$ , all channels ON		12.8	15.6	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	$^\circ\text{C}$
$t_{HYS}$	Hysteresis			15			$^\circ\text{C}$

**SWITCHING CHARACTERISTICS**
 $V_{CC} = 5\text{ V}$ ,  $T_J = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output from $\overline{G}$	$C_L = 30\text{ pF}$ , $I_D = 48\text{ mA}$		210		ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from $\overline{G}$			75		ns
$t_r$	Rise time, drain output			250		ns
$t_f$	Fall time, drain output			200		ns
$t_{pd}$	Propagation delay time, SRCK $\downarrow$ to SEROUT	$C_L = 30\text{ pF}$ , $I_D = 48\text{ mA}$		35		ns
$T_{or}$	SEROUT rise time (10% to 90%)	$C_L = 30\text{ pF}$		20		ns
$T_{of}$	SEROUT fall time (90% to 10%)	$C_L = 30\text{ pF}$		20		ns
$f_{(SRCK)}$	Serial clock frequency	$C_L = 30\text{ pF}$ , $I_D = 20\text{ mA}$			10	MHz
$T_{SRCK\_WH}$	SRCK pulse duration, high		30			ns
$T_{SRCK\_WL}$	SRCK pulse duration, low		30			ns

DEVICE INFORMATION

PIN CONFIGURATIONS

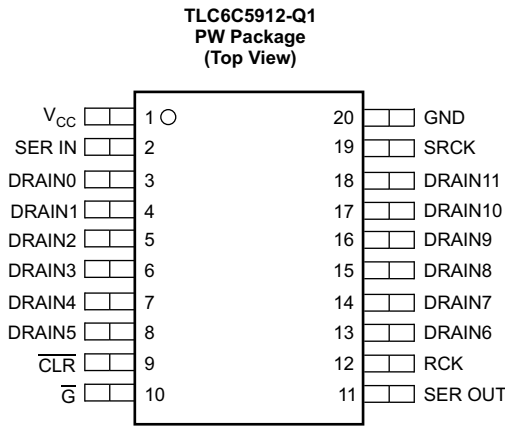


Figure 3. PW-Package Pin Configuration of TLC6C5912-Q1

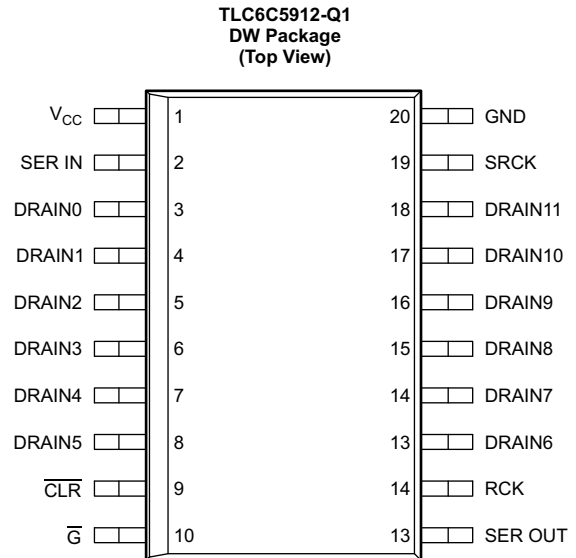


Figure 4. DW-Package Pin Configuration of TLC6C5912-Q1

PIN FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
CL $\bar{R}$	9	I	Shift register clear, active-low
DRAIN0	3	O	Open-drain output
DRAIN1	4	O	Open-drain output
DRAIN2	5	O	Open-drain output
DRAIN3	6	O	Open-drain output
DRAIN4	7	O	Open-drain output
DRAIN5	8	O	Open-drain output
DRAIN6	13	O	Open-drain output
DRAIN7	14	O	Open-drain output
DRAIN8	15	O	Open-drain output
DRAIN9	16	O	Open-drain output
DRAIN10	17	O	Open-drain output
DRAIN11	18	O	Open-drain output
$\bar{G}$	10	I	Output enable, active-low
GND	20	-	Power ground
RCK	12	I	Register clock
SER IN	2	I	Serial-data input
SER OUT	11	O	Serial-data output
SRCK	19	I	Shift-register clock
V <sub>CC</sub>	1	I	Power supply

## PIN DESCRIPTIONS

$\overline{\text{CLR}}$  is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear CLR is high. Driving  $\overline{\text{CLR}}$  is low clears all the registers in the device.

**DRAIN0–DRAIN11** are the LED current-sink channels. These pins connect to the LED cathodes, and they can survive up to 40-V LED supply voltage. This is quite helpful during automotive load-dump conditions.

$\overline{\text{G}}$  is the LED channel enable and disable input pin. Having  $\overline{\text{G}}$  low enables all drain channels according to the output-latch register content. When high, all channels are off.

**GND** is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.

**RCK** is the storage register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable  $\overline{\text{G}}$  input signal is high.

**SER IN** is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

**SER OUT** is the serial data output of the 12-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.

**SRCK** is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.

**V<sub>CC</sub>** is the power supply pin voltage for the device. TI recommends adding a 0.1  $\mu\text{F}$  ceramic capacitor close to the pin.

## THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device begins to operate again.

### APPLICATION INFORMATION

Figure 5 shows a typical cascade application circuit with two TLC6C5912-Q1 chips configured to cascade topology. The MCU generates all the input signals.

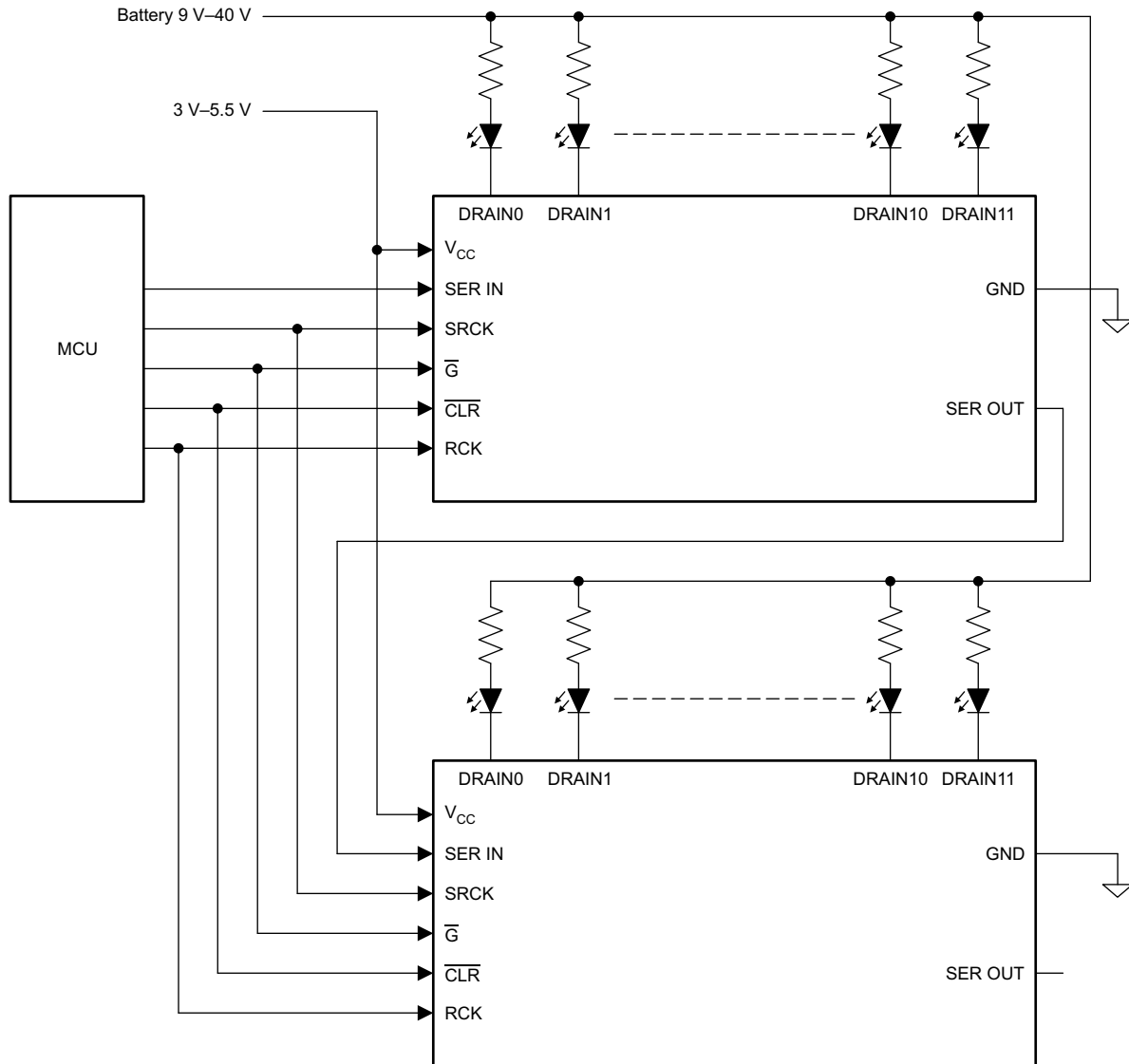
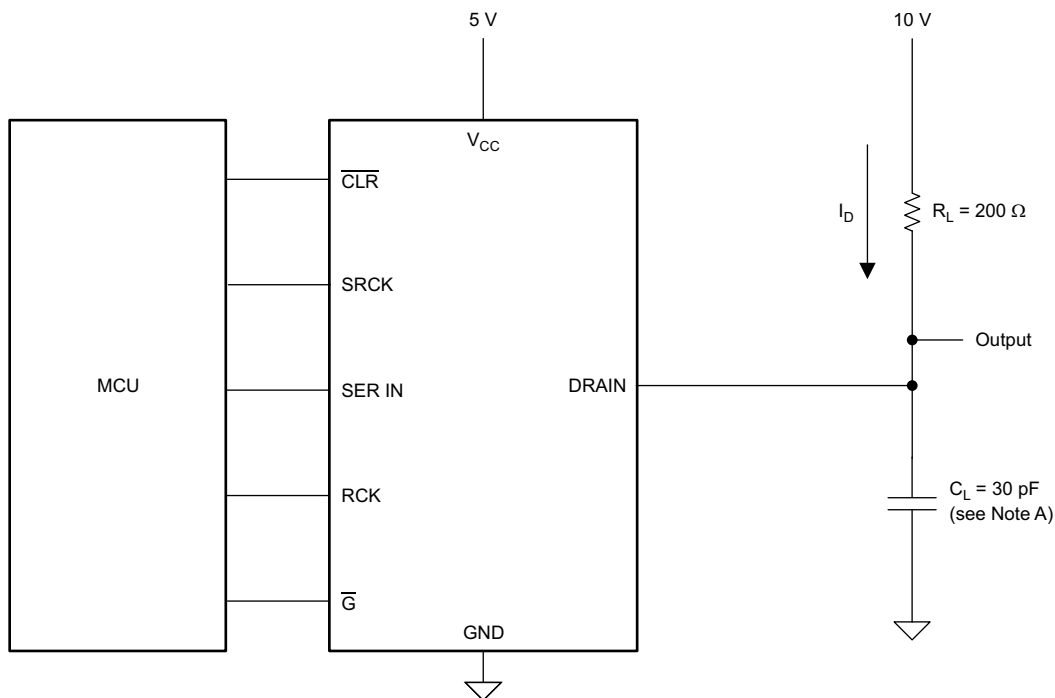


Figure 5. Typical Application Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 6. Resistive-Load Test Circuit

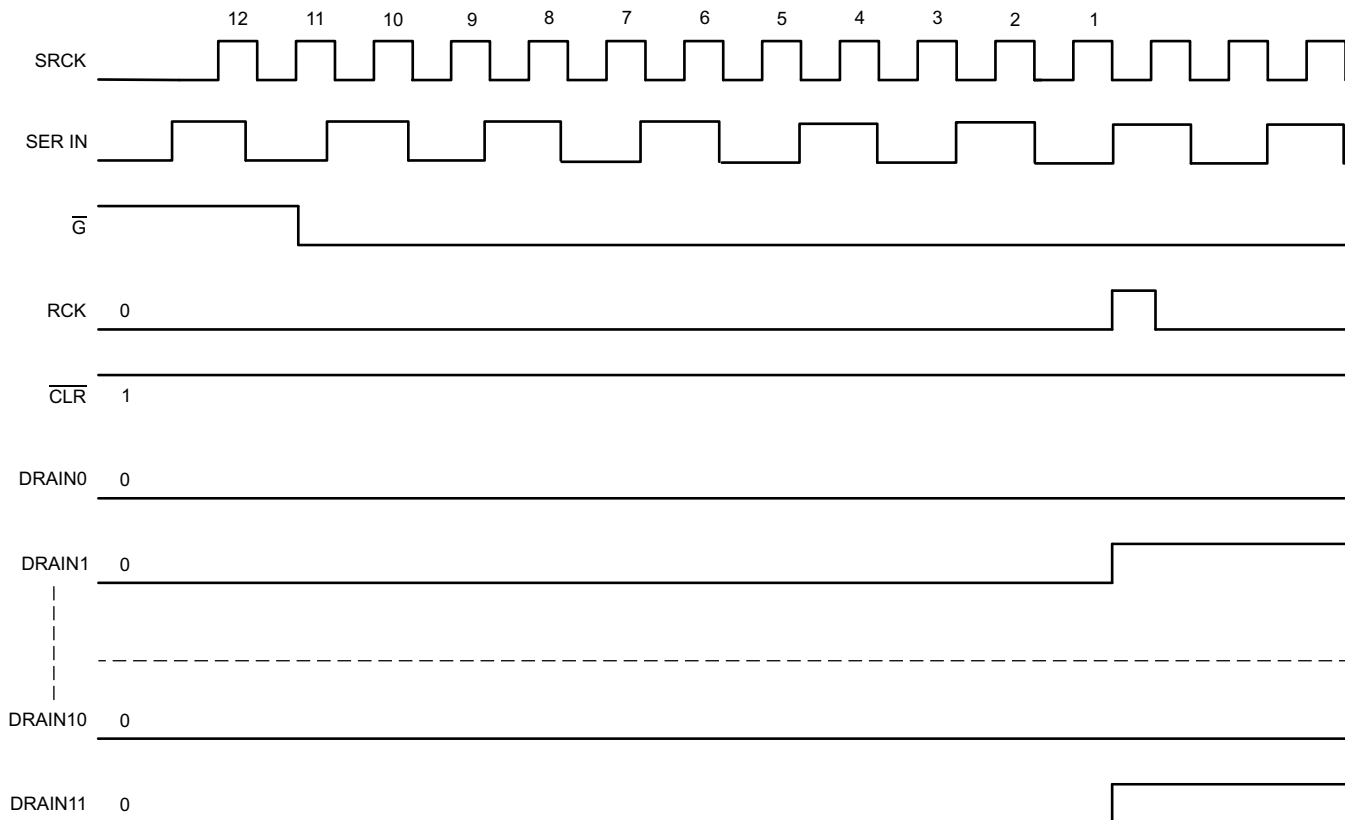
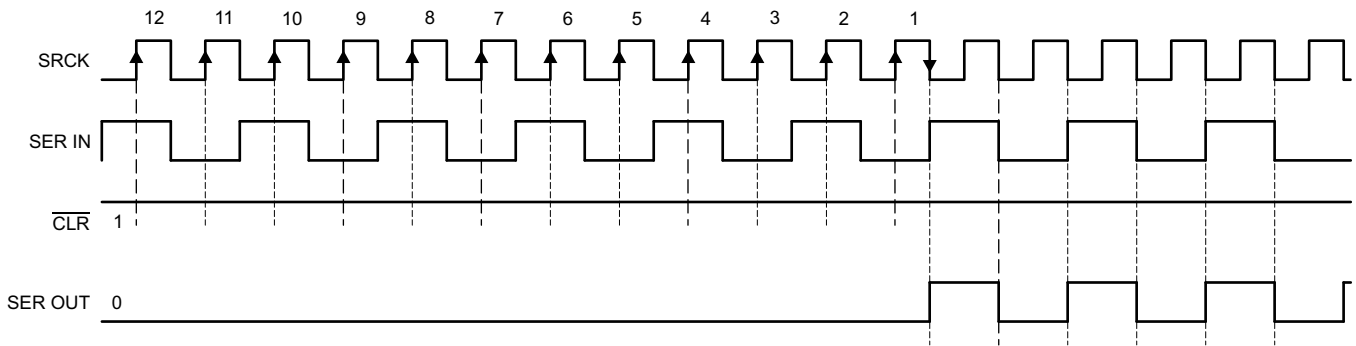


Figure 7. Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)**

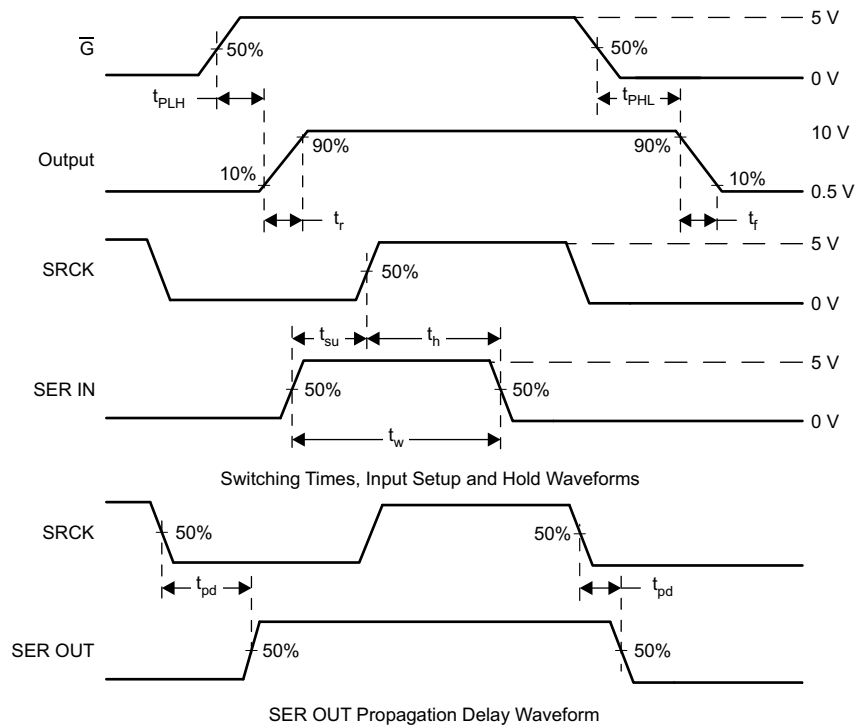
Figure 6 and Figure 7 show the resistive-load test circuit and voltage waveforms. One can see from Figure 7 that with  $\overline{G}$  held low and  $\overline{CLR}$  held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.

**TIMING WAVEFORM**



**Figure 8. SER IN to SER OUT Waveform**

Figure 8 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.



**Figure 9. Switching Times and Voltage Waveforms**

Figure 9 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 7.

TYPICAL CHARACTERISTICS

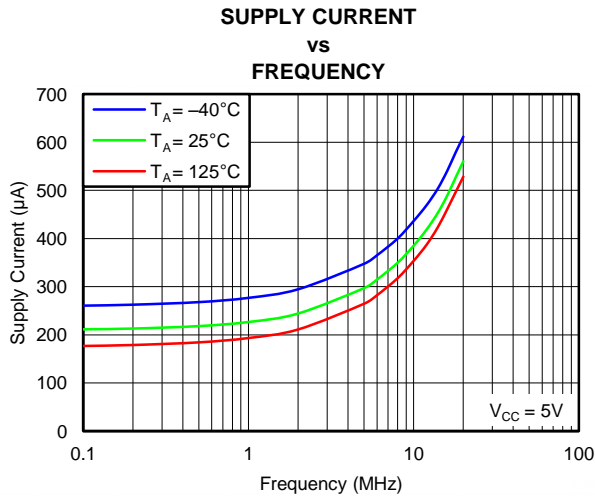


Figure 10.

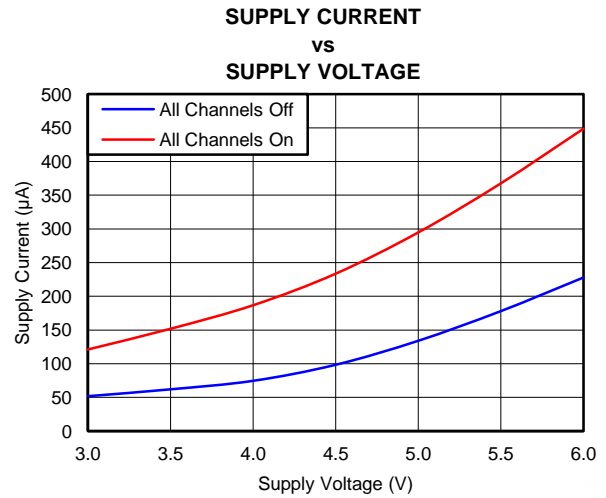


Figure 11.

Conditions for Figure 12 and Figure 13: Single channel on

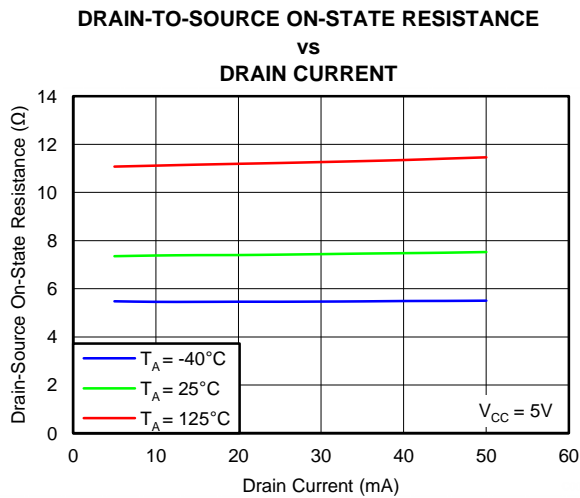


Figure 12.

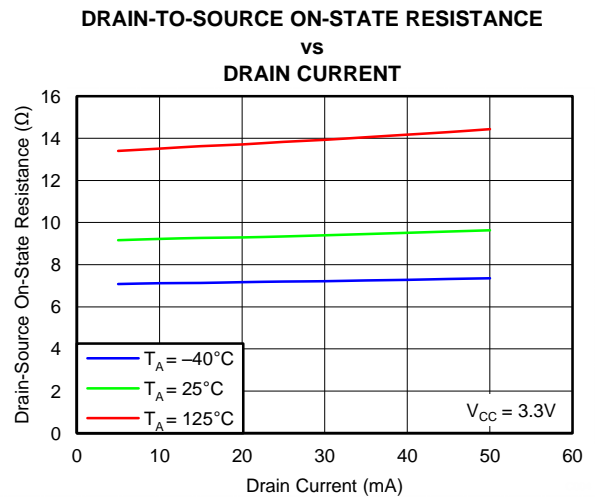


Figure 13.

### TYPICAL CHARACTERISTICS

Conditions for Figure 14, Figure 15, and Figure 16: All channels on

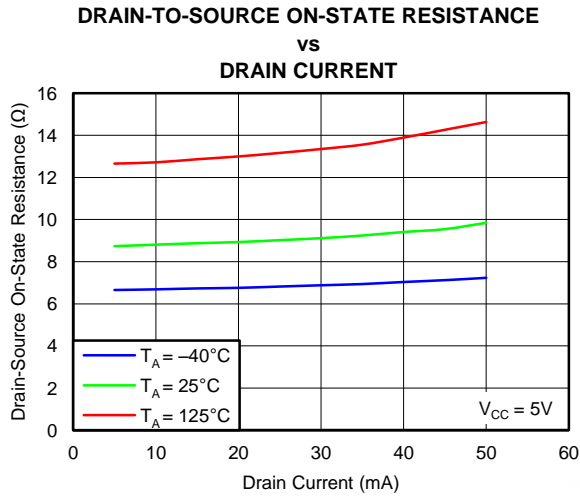


Figure 14.

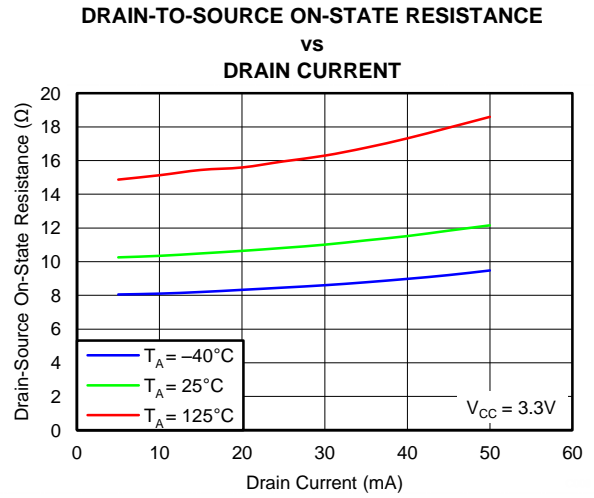


Figure 15.

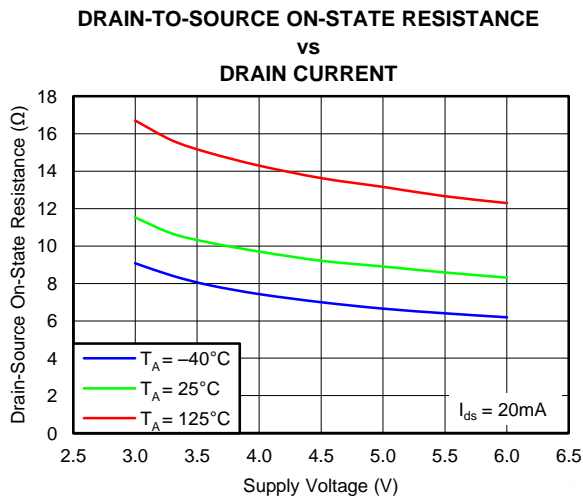


Figure 16.

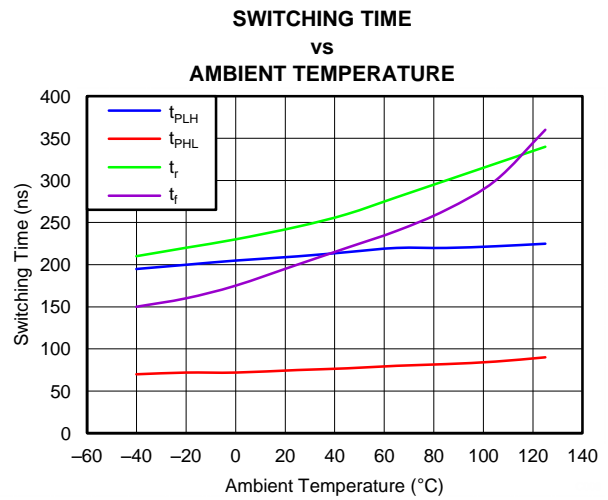


Figure 17.

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**REVISION HISTORY**

<b>Changes from Original (December 2012) to Revision A</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed the device From: Product Preview To: Production .....</li></ul> <hr/>	<hr/> <b>1</b> <hr/>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC6C5912QDWRQ1	PREVIEW	SOIC	DW	20	2000	TBD	Call TI	Call TI	
TLC6C5912QPWQ1	PREVIEW	TSSOP	PW	20	70	TBD	Call TI	Call TI	
TLC6C5912QPWRQ1	PREVIEW	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.



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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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